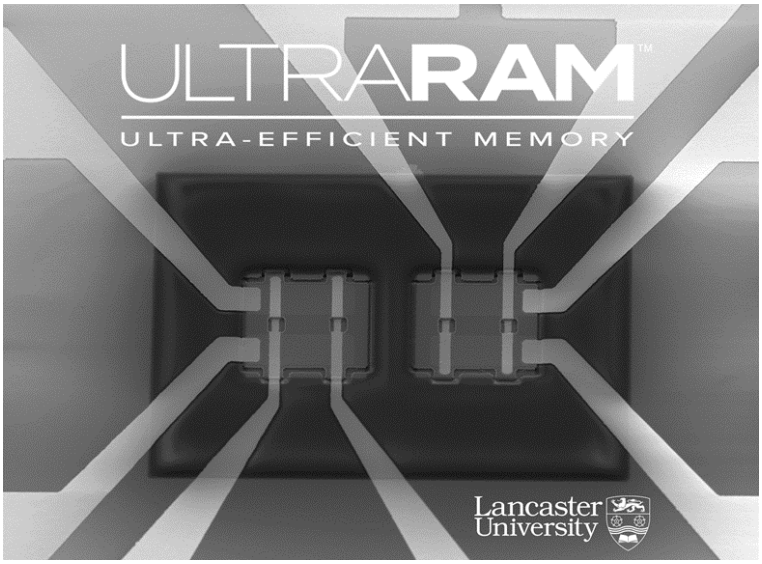
ULTRA**RAM™: A High-performance, Ultra-efficient, Non-volatile, Random-access Memory**

Professor Manus Hayne

Department of Physics, Lancaster University, Lancaster LA1 4YB, United Kingdom

With 2019 sales of $106 bn, memories are (almost) equally matched with logic in terms of the market size.[1] However, in contrast to logic, which is a monolith of a single technology, Si CMOS, there are four 'conventional' memories, SRAM, DRAM, NAND and NOR flash, only one of which (SRAM) has CMOS as its fundamental basis. Furthermore, there is vibrant research activity into new forms of memory, usually called emerging memories, including phase change RAM, resistive RAM, and spin-transfer torque magnetic RAM.[2,3] These emerging memories aspire to combine the non-volatility of flash with the performance of DRAM, and some are available commercially, *e.g.* Optane™. With this in mind, there is clearly scope for innovative memory research, and realistic prospects of commercialisation.

In this talk I will introduce a novel charge-based memory,[4] ULTRA**RAM**™, which exploits the ability of a triple-barrier resonant tunnelling (TBRT) structure to switch from opaque to transparent on application of ≤2.5 V, allowing a memory that combines the contradictory properties of non-volatility (flash-like) with fast, low-energy switching (DRAM-like).[5,6] The talk will be divided into four parts. In the first part I will briefly introduce the research environment in Lancaster and my team. In Part II I will explain the physics behind the TBRT concept and describe the results of first generation (Gen I) devices. Part III will then go on to present the further innovations that resolve issues in Gen I devices, and allow the implementation of a highly compact architecture suitable for arrays. Part IV details planned research to allow large-volume manufacture of ULTRA**RAM**™ memory chips; large arrays, development and integration of III-V CMOS for addressing, implementation on Si substrates and device scaling.



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